Remarks

Claims 1-11 are pending in the application. Claims 1-7 stand rejected and claims 9 and 11 are allowed. By this amendment claim 1 has been amended. Applicants respectfully request consideration of Applicants' response herein.

Claim Rejections - 35 U.S.C. § 102(b)

The Examiner rejected claims 1-7 under 35 U.S.C. § 102(b) as being anticipated by U.S Patent No. 6,373,779 to Pang. The Examiner stated that Pang discloses "a method for accessing memory cells (Fig. 3) within a memory array operated with a precharge mechanism, in which differential read and write access operations are performed by activating a true bitline and a complement bitline," citing Fig. 5, Column 5, lines 30-67, Col. 6, lines 1-4; "determining whether a next memory access operation is a read access operation or a write access operation," citing Col. 5, lines 38-46; and "performing a precharge of the true and compliment bitlines only when a read access operation follow the current access operation, citing Col. 5, lines 30-38 and 60-67, Col. 6, liens 17-25.

Applicants respectfully submit that Pang is directed to a dual port RAM employing a plurality of write modes that may be selectively and independently programmed for each port. (Pang, Abstract, Col. 3, lines 42-47) In Figs. 6, 7 and 8, Pang discloses the switching activities associated with the operation of each write mode occurring over a single clock cycle. In this regard, Pang does not anticipate disabling a bitline precharge based on whether the next memory operation in a subsequent clock cycle will be a read access. Pang is intended to provide greater flexibility in writing to a configuration memory integral to a programmable logic device and not to a method to limit bitline precharge switching activity based on an anticipated next memory access operation in a subsequent clock cycle.

Applicants' method is directed to reducing power dissipation from unnecessary precharging of memory bitlines following a write access. In other words, Applicants' method contemplates precharging the bitlines of the memory only when a read access follows the current access operation. (Applicants' Specification at paragraph 11, claim 1.) When a write access follows the current access operation, Applicants' precharge circuitry is disabled. (Applicants' Specification at paragraph 11, claim 1.) As such, Applicants respectfully submit that the method claimed herein is not anticipated or suggested by Pang.

The Examiner cited the operation of Pang's bitline precharge at Col. 6, lines 43-45, which merely observes that the precharged complimentary bitline pair is coupled to the sense amplifier in "preparation for the next access." Pang does not address or disclose a method to determine whether the next memory access occurring in a subsequent clock cycle is a read or write access as claimed herein. Instead Pang focuses on switching activities within a single clock cycle, which is clearly shown in Figs. 5-8 because the clock signal level never changes after the first rising edge. Indeed, the description of various logical dependencies and associated switching activity cited by the Examiner occurs within a single clock cycle and does not anticipate a method in which the memory access operation for a next clock cycle is determined, nor does Pang disclose disabling a bitline precharge function based on whether the next access is a read operation.

Similarly, the text cited by the Examiner at Col. 6, lines 38-50 describes the deassertion of the sense amp enable signal and coupling of the precharged bit line pair for the next access as is common in prior art SRAMs. (Pang at Col. 6, lines 38-50) Applicant's respectfully submit the text cited by the Examiner does not anticipate or suggest a method for inhibiting a bit line precharge to reduce power dissipation. Further, Pang does not disclose nor claim a memory array having a read cycle signal controller for generating a read cycle (n+1) signal when a next memory access operation is a read access operation, nor does Pang logically evaluate the first precharge control signal and the read cycle control (n+1) signal to determine whether a next memory access is a read access operation for gating the precharge circuit. (Applicants' Specification, paragraphs 11-13, claim 8.) To clearly illustrate this temporal distinction, Applicants have amended claim 1 to recite: "determining whether a next memory access operation occurring <u>in a clock cycle</u> subsequent to an

access operation occurring in a current clock cycle is a read access operation or a write access operation..."

In addition, Applicants' describe a mode of operation in which the latency required to evaluate whether the n+1 cycle will be a read access is generated by adding an extra clock cycle to the memory access time. (Applicants' Specification at paragraph 30, claim 7.) As such, the methodology claimed by Applicants emphasizes the stated objective of saving power at the expense of performance, which is similarly not anticipated by Pang.

At Col. 6, lines 6-20, Pang describes the function of a conventional sense amplifier for SRAM applications: "As a result, the voltages on BL and BL# are precharged and equalized in preparation for the next access." (Col. 6, lines 24-26) Again at Col 6 lines 40-49, Pang describes the bitline pair being coupled to the sense amplifier to conclude the read operation. Applicants respectfully submit that Pang does not consider the issue of power dissipation associated with precharge operations and therefore does not disclose a method for inhibiting a bit line precharge to when a next memory access will be a read access.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. (MPEP §2131) Applicants respectfully submit that Pang does not teach or suggest Applicants' method of limiting bit line precharge to access operations in which the next access operation is a read access. Similarly, Pang does not anticipate the element of disabling a precharge operation when data are written in the next memory access cycle nor of incurring a memory performance penalty to reduce power dissipation associated with bitline precharge operations. Therefore Pang does not anticipate every element of Applicants' claimed method. Claims 2-7 depend from claim 1 as amended. Therefore, Applicants respectfully submit that the Examiner's rejection of claims 1-7 under 35 U.S.C. § 102(b) has been overcome.

Allowable Subject Matter

Applicants gratefully acknowledge the Examiner's indication of allowed claims 9-12 in the Office Action Summary and note that Applicants previously amended claims 9 and 10 to include all the limitations of the base claim and any intervening claims to overcome the Examiner's objection and are therefore in condition for allowance.

Prior Art Made of Record

The prior art made of record by the Examiner and not relied upon, i.e. Yap, Chang-Cheng, et al. (U.S. Patent App. No. 2005/0125596), has been reviewed and Applicants respectfully submit that the references cited do not anticipate or suggest the elements of pending independent claim 1.

Conclusion

Based on the foregoing, it is respectfully submitted the application may be passed to issuance.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

Respectfully submitted,
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